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New LDMOS Model Delivers Powerful Transistor Library—*Part 2: Library Applications*

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The conclusion of this 2-part article shows that the CMC model can be scaled for a larger device, with a good fit for signal, power and distortion performance—illustrated by a 60 watt Doherty power amplifier design example

Last month, Part 1 of this article introduced the new CMC (Curtice/Modelithics/Cree) non-linear LDMOS FET transistor model. The CMC model was described, and its utility demonstrated by making extractions on a 1 watt wafer-probeable FET.

In Part 2, this device is used as the core of a 30 watt model to show the scalability to larger devices. The 30 watt model is built up by adding appropriate package parasitics and thermal model parameters to a scaled version of the 1 watt cell model and then validated against linear and non-linear measurement data. A 19 element high power transistor library based on the CMC model is also explained. This library covers devices of various power levels up to 90 watts and frequencies over the DC to 2.7 GHz range.

As an example of the good results that can be achieved with the new model library, a 60 watt UMTS band Doherty amplifier, employing the CMC UGF21030 LDMOS FET model, has been designed, achieving excellent efficiency and linearity simultaneously, with simulation-to-measurement agreement far exceeding that achieved with models available previous to the CMC.

Modeling of a 30 Watt Packaged LDMOS FET Transistor

The die used in the 30 watt Cree UGF21030 transistor has the same cell layout as employed in the 1 watt FET. A major feature of the CMC model is that it has been found to scale very well with increasing gate width through the use of the AREA parameter. In developing the UGF21030 model, this feature was used to scale the 1 watt core device model to 30 watts. Next, the thermal resistance was changed, using the R_TH parameter, to include the heat-sinking effects of the package and finally, the package model was developed.

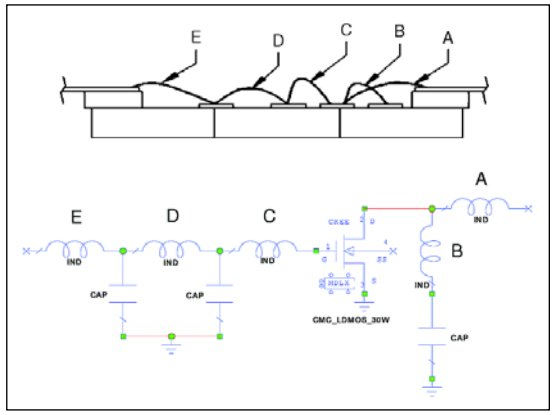

Figure 1 · Partioning of parasitic elements.

The package modeling approach adopted was to measure and calculate the parasitic capacitances of the package and to calculate the wire-bond inductances of the internal matching structures. The bond wire inductances were calculated to include any mutual coupling effects. Figure 1 shows the partitioning of the parasitic elements in comparison with the physical positioning of the die.

With the complete package model in place, the element values were then refined by comparing simulated data with measured *S*-parameter and load pull data. Resistive losses were also added at this point. The transmis-

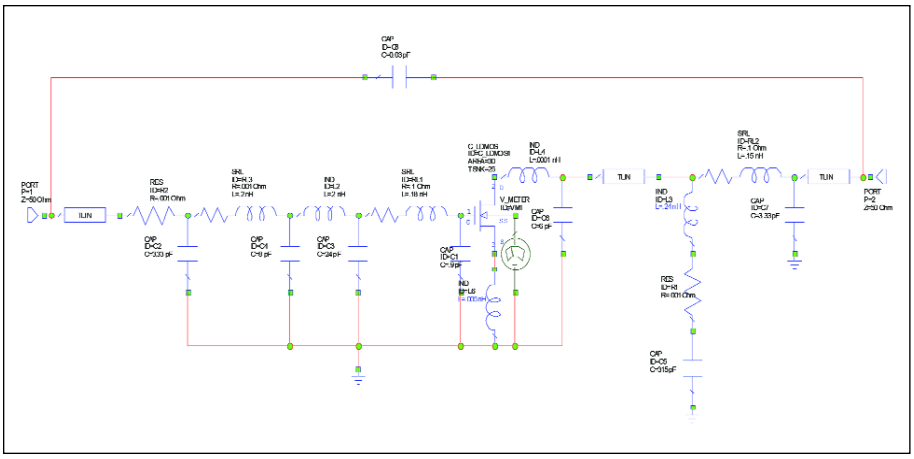

Figure 2 · Full UGF21030 Model including all parasitic elements.

sion line elements, as seen in Figure 2, were included to compensate for measurement reference plane issues associated with the drain wire bond manifold and the package bond shelf.

The small signal *S*-parameter fits of the modeled UGF21030 transistor versus measured data over the frequency range of 0.5 to 3.0 GHz are shown in Figure 3. In the following comparative plots measured results are displayed in red and modeled results in blue. It can be seen that the S_{11} and S_{22} fits are very good over a broad bandwidth. The Smith chart plots show that the resonant frequencies of the input and output matches are well modeled. This was found to be of particular importance in achieving agreement with load-pull data. The differences in S_{21} values between measurement and model with frequency are likely due to overly simplistic bond wire models that do not exactly model the mutual coupling effects. The distributed nature of the large aspect ratio matching capacitors is also now known to be causing some of this dispersion.

The simulated load-pull contours for the UGF21030 model are shown in Figure 4. These were generated using the Microwave Office™ "load-pull wizard."

The optimum measured impedance points have been displayed on the Smith chart using the LPCMMAX function. These were measured using the Maury Microwave ATS automated load pull system, again excellent agreement can be observed. The performance of the UGF21030 model in terms of swept power was verified against data sheet curves by simulating power, gain, power added efficiency (PAE) and linearity with the device model presented with the optimum measured source and load impedances. The simulated data is shown in Figures 5 and 6 with a comparison against the measured data presented in Table 1. The crosses in Figure 6 indicate measured data points.

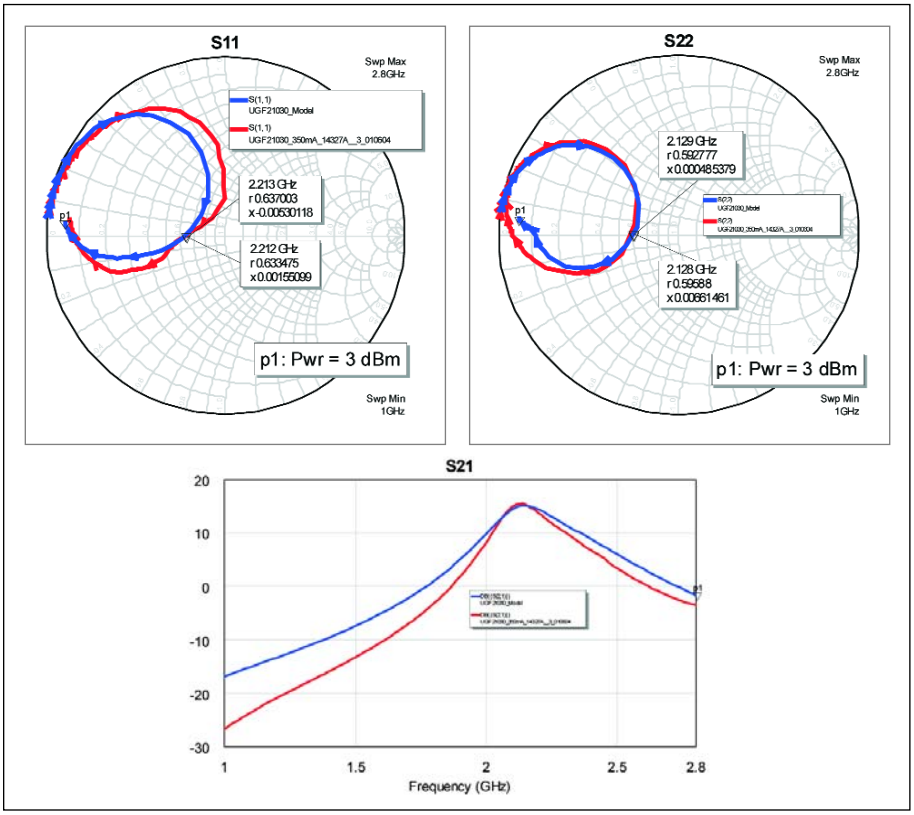

Figure 3 · Fits to *S*-parameter data for UGF21030 from 1 GHz to 2.8 GHz, V_{dd} = 28 V, I_{dq} = 350 mA

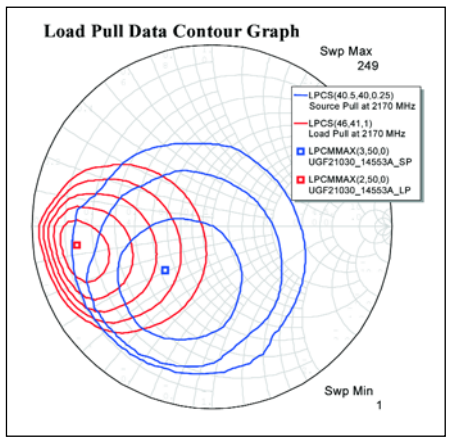

Figure 4 · Simulated load and source pull contours and measured optimal impedances at 2.14 GHz, V_{dd} = 28 V, I_{dq} = 350 mA.

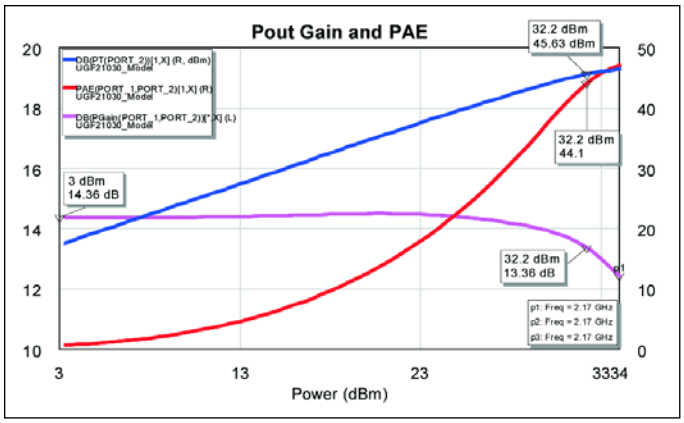

Figure 5 · Simulated power output, gain and PAE at 2.14 GHz, V_{dd} = 28 V, I_{dq} = 350 mA.

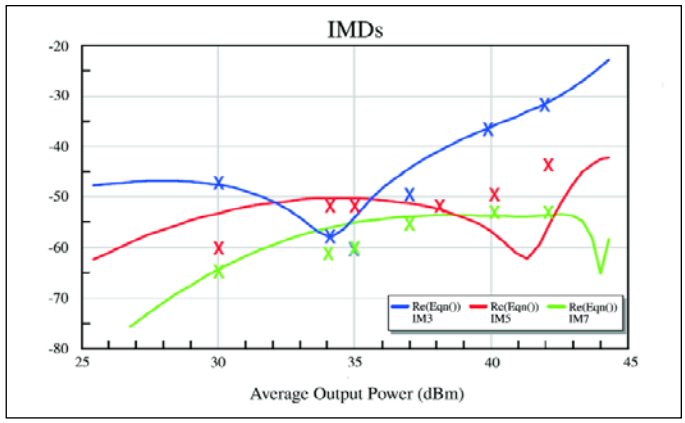

Figure 6 · Intermodulation distortion performance at 2.14 GHz, V_{dd} = 28 V, I_{dq} = 350 mA.

Parameter	Simulated	Measured
P_{1dB} (dBm)	45.63	45.4
Gain (dB)	13.36	13.65
PAE (%)	44.1	44.0

Table 1 · Comparison of measured and simulated performance for UGF21030.

A New High Power LDMOS Model Library

The UGF21030 model (and its evolution) has been shown as an example of the CMC models available in the new Cree Microwave LDMOS FET model library. This new model library can be accessed at the following Web address:

http://www.modelithics.com/vendor_models/Cree.shtml

The model library currently consists of 19, fully validated, high accuracy, non-linear transistor models ranging in power levels from 5 to 90 watts for circuit applications to 2.7 GHz. In developing these models similar scaling, thermal resistance adjustment package modeling and measurement validations have been performed. In addition all models have been tested against a rigorous quality assurance procedure and each model is provided with a data sheet outlining the model's performance.

Successful Design and Realization of a 60 Watt Doherty Power Amplifier

The design of low power (<10 watt) Doherty amplifiers at microwave frequencies using classical formulae to calculate the required output impedances has been well documented [1], [2]. The analysis has also been extended to more complex topologies such as N-Way [3], [4]. Owing to the relatively low RF power levels and, therefore, the correspondingly low parasitic effects in the transistors the "classical" equations work well resulting in first time design success. When designing a Doherty amplifier at higher power levels it is important to realize that the impedances that must be matched for correct Doherty operation are no longer purely real, but have significant imaginary parts. An accurate large signal transistor model allows the achievement of first time design success. Preliminary work used a SPICE-based model [5]. Whilst this model made good predictions of power, gain and efficiency (both at compression and at back-off) it was found to be insufficient in modeling the sub-threshold region for accurate predictions of backed-off linearity. In a Doherty amplifier it is even more critical that the sub-threshold regions be modeled accurately as the peaking amplifier (or amplifiers in an N-Way configuration) operates in this area of the I-V space being biased in Class B mode. Modeling of the small signal response is also affected.

A 60 watt UMTS band Doherty amplifier, employing the CMC UGF21030 LDMOS FET model, has been designed achieving excellent efficiency and linearity simultaneously. All large signal simulation work was performed in Applied Wave Research Microwave Office (MWO). Layout sensitive elements of the design were analyzed using Momentum™ from Agilent Technologies. The design methodology was as follows:

1. Single ended circuit modeling
2. Doherty circuit design
3. Manufacture and test of prototypes

The first stage of single ended circuit modeling was to use the "load-pull wizard" in MWO to generate large signal source and load impedance data across the band of interest as a starting point for the circuit synthesis. The matching networks were then designed as basic LC equivalents in a third party visualization tool. The LC networks were next entered into the MWO environment and transformed into a model of

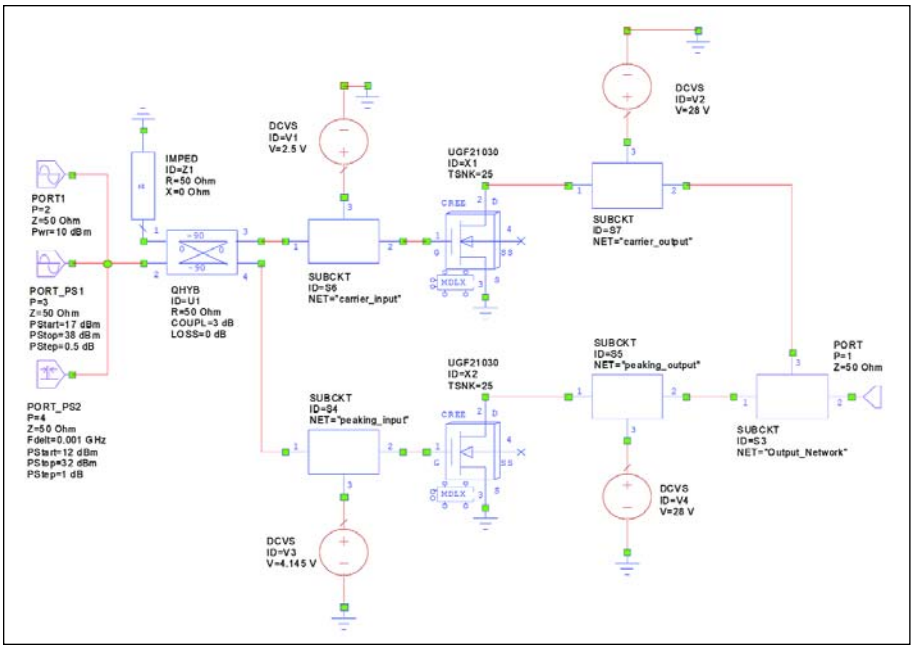

Figure 7 · Complete Doherty amplifier model.

real transmission lines and capacitors. Any transmission lines with *w/h* ratios outside of the bounds of classical equations were analyzed using Momentum, which is a 2.5D electromagnetic simulator. The input and output networks were then combined with the UGF21030 CMC model and optimized as a 50-ohm class AB amplifier.

The Doherty amplifier combining networks were then designed and the complete amplifier circuit was optimized starting with the 50-ohm class AB amplifiers as building blocks. Extra phase lengths were added to enable transformations to the correct impedances [6]. The complete amplifier circuit was then load-pulled to ensure that optimum performance had been achieved. The top-level circuit schematic is shown in Figure 7.

The schematic shows three different input ports set up for convenience to allow all facets of the design to be inspected. The input and output matching blocks for the peaking and carrier amplifiers are all unique. They consist of the final microstrip elements and *S*-parameter blocks generated from the planar electromagnetic simulator. The input divider used was an Anaren Xinger™, which is modeled as an ideal element with about 0.2 dB loss. This was found to be sufficient for this work. It should be noted that an *S*-parameter block may seem a more accurate alternative but the upper frequency of the available data files is 6 GHz. This can be a source of error when performing harmonic balance simulations, as the higher order harmonics will be in an extrapolated region of the *S*-parameter data.

The circuit was realized using a 31 mil thick, PTFE fiberglass board, which was sweat soldered to an aluminum plate for good grounding and heat sinking. The transistors were clamped into the circuit. A photo of the final amplifier can be seen in Figure 8.

The 60 watt Doherty amplifier was evaluated under a number of different stimuli. In the following comparative plots the data markers represent the measured data, whereas the solid lines represent the simulated data. The small signal gain of the amplifier was measured from 1.5 GHz to 3 GHz. A comparison of the measured and modeled results can be seen in Figure 9. The prediction of the nulls either side of the pass band is excellent. The upper null is attributable to the peaking amplifier. This fit can only be achieved using a model that works well in the subthreshold region.

The amplifier was measured over

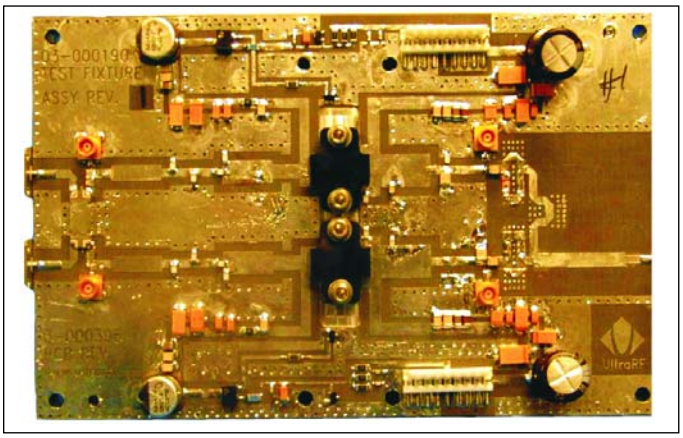

Figure 8 · 60 watt Doherty amplifier prototype.

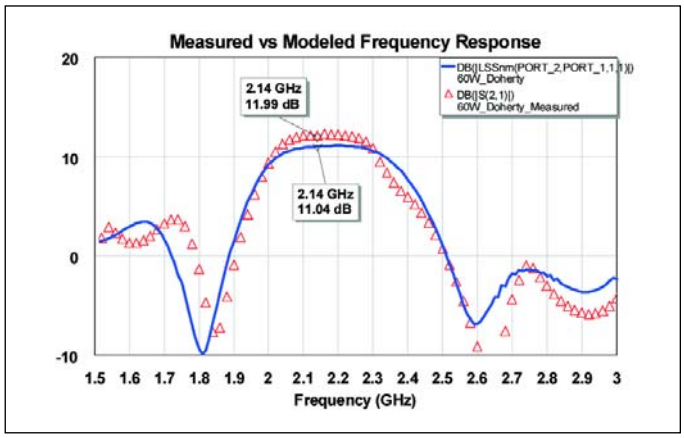

Figure 9 · Small signal results.

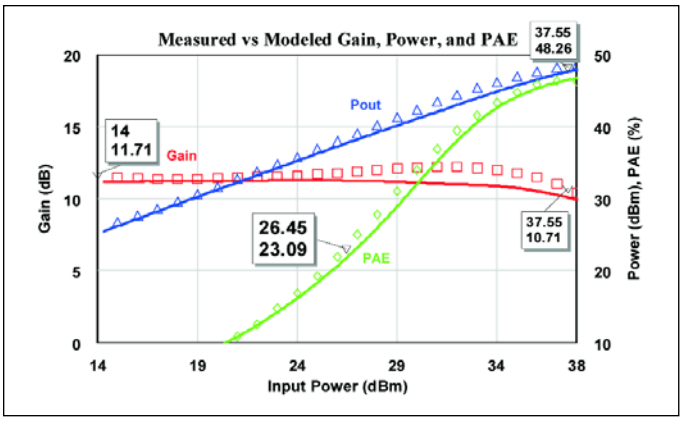

Figure 10 · Large signal power sweep.

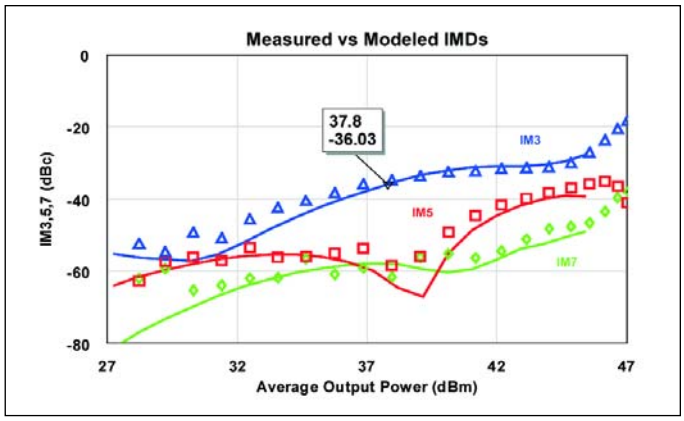

Figure 11 · Intermodulation results.

a 25 dB dynamic range with gain, power and efficiency curves plotted simultaneously. These curves are presented in Figure 10. It is interesting to note that the efficiency curve, both modeled and measured, does not show a very strong Doherty shape. Without a model this may have been cause for concern as to whether the amplifier had been correctly implemented. It is however predictable and is a function of the high power level and linearity target.

Swept power measurements were made using an Anritsu Power Amplifier Test System (PATS™). The linearity of the amplifier was also measured using the PATS. The third, fifth and seventh order intermodulation distortion products were observed over 20 dB of dynamic range. Data is presented in Figure 11. The prediction of the nulls in the responses is excellent.

Whilst this is a very fast measurement with all curves displaying simultaneously the system noise floor is compromised. This can be seen in the level of the IMDs at low power. The simulation has a superior noise floor predicting seventh order products to better than –80 dBc. The amplifier was also evaluated under two-carrier W-CDMA test signals and met an ACLR specification of –35 dBc at 6 watts average output power with a drain efficiency of 23%. The spectral plot is shown in Figure 12.

Conclusions

A powerful new large signal LDMOS FET model has been developed and, shown to scale well in translating from die to larger packaged devices. The model has enabled a very versatile library of high power transistor models addressing powers to 90 watts and frequencies to 2.7 GHz.

Library model accuracy has been demonstrated in a complex application that requires all regions of DC and RF operation to be well modeled. The results of this work show excellent agreement between simulations and measurements of the complete Doherty amplifier. Of considerable importance is the fact that the transistor model is capable of providing wide band simulations.

The model has also provided further insight into the operation of higher power Doherty amplifiers and has highlighted some of the sensitivities of these designs. The number of variables in the Doherty amplifier makes practical tuning methods ineffective. Having an accurate large signal model allows the power amplifier designer to engineer more complex architectures with confidence.

Acknowledgements

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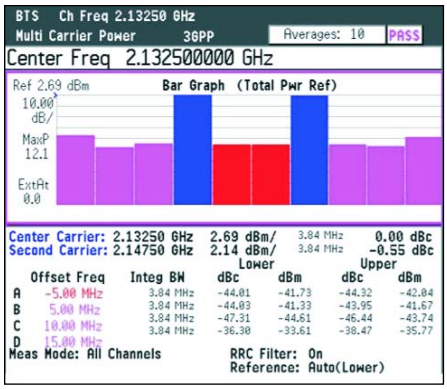

Figure 12 · W-CDMA result at P_{ave} = 6 W.

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Additonal information on LDMOS FET devices and the availability of the models described in this article can be obtained from either of these companies:

Cree Microwave, Inc.
Sunnyvale, CA
Tel: 408-962-7783
www.creemicrowave.com

Modelithics, Inc.
Tampa, FL
Tel: 813-866-6335
www.modelithics.com

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